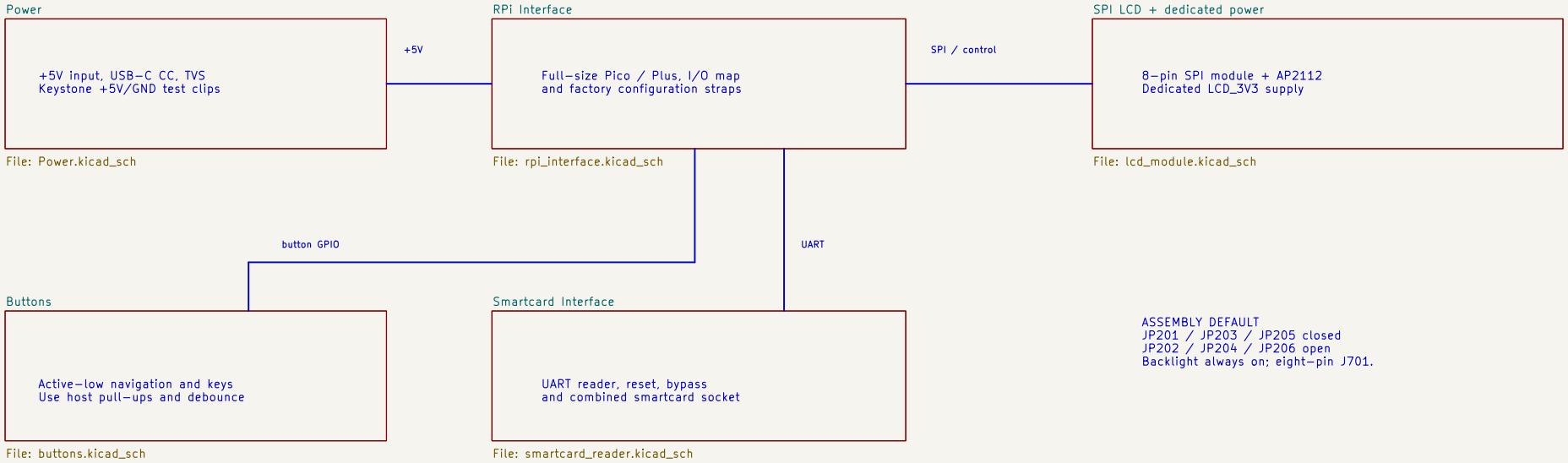
ShieldSigner | eight-pin pill carrier

Native KiCad reference | 160 x 70 mm | four copper layers | 1.6 mm nominal thickness

READING MAP (lines below describe system flow; connections use named nets on the circuit sheets)



ASSEMBLY DEFAULT
JP201 / JP203 / JP205 closed
JP202 / JP204 / JP206 open
Backlight always on; eight-pin J701.

STACKUP / REVIEW
F.Cu signals / In1.Cu GND / In2.Cu GND / B.Cu signals. Confirm the nominal stackup with the fabricator.
0.0.13-dev uses nine factory service points and four independent M2.5 bracket anchors.
ERC / DRC are software checks. Module fit, powered operation and supplier assembly remain unqualified.

Prototype: physical fit, powered operation and assembly not qualified
Derived from 3rdIteration/SeedSigner; original design: Stephen Rothy
ShieldSigner / LightningSpore

Sheet: /
File: SeedSigner-Plus-smartcard-pico.kicad_sch

Title: System overview and reading map

Size: A4	Date: 2026-11-08	**Rev: 0.0.13-dev**
KiCad E.D.A. 10.0.7		Id: 1/6

Host module, signal mapping and assembly straps

U202 is the customer-fitted Pico interface; J203/J204 are the two factory SMT strips.
U201 is a schematic-only legacy reference, not a factory assembly part.

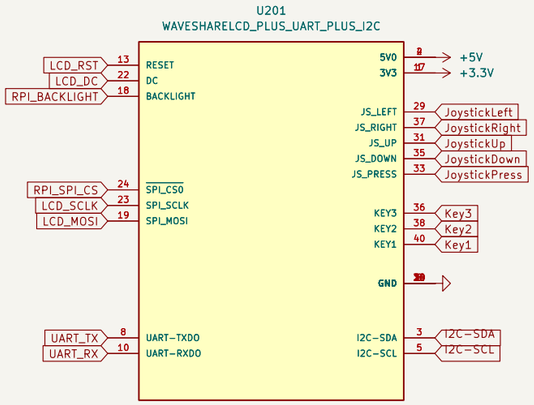
BACKLIGHT: default high



CHIP SELECT: default GPIO

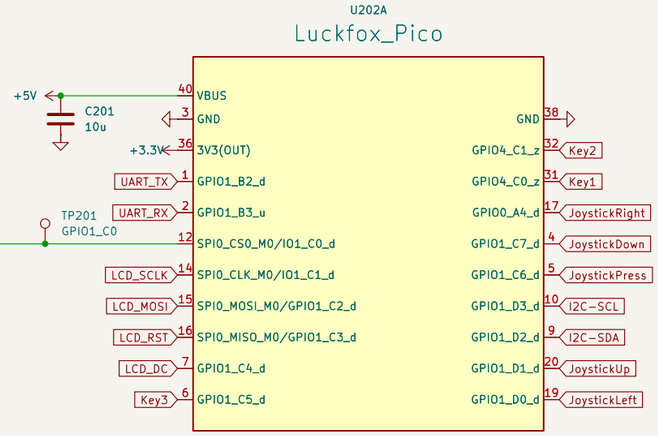


LEGACY INTERFACE REFERENCE ONLY
U201 and TP201 have no PCB footprint.



GPIO1_C0 FUNCTION



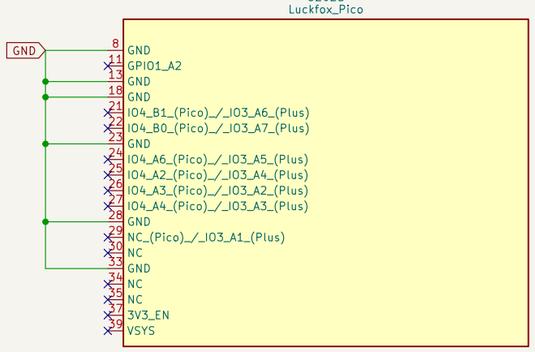


FACTORY STRAP TABLE
JP201 closed / JP202 open: backlight held high
JP203 closed / JP204 open: GPIO1_C0 drives CS
JP205 closed / JP206 open: GPIO-controlled CS
Never close both alternatives in a strap pair.

BACKLIGHT SOURCE
JP202 selects MCU_BACKLIGHT only in an alternate configuration.
This PCB has no dedicated host PWM path; use the separate PWM candidate.

HOST FIRMWARE
Use the carrier GPIO map and 320 x 240 display profile.
The 240 x 240 bench image conflicts with two button nets.

Unused full-size header positions



Factory J203/J204: 2x XKB C2883777 SMT male strips.
Pico underside: 2x M20-7822042 female sockets; no adapter.

Prototype: physical fit, powered operation and assembly not qualified
Derived from 3rdIteration/SeedSigner; original design: Stephen Rothy
ShieldSigner / LightningSpore

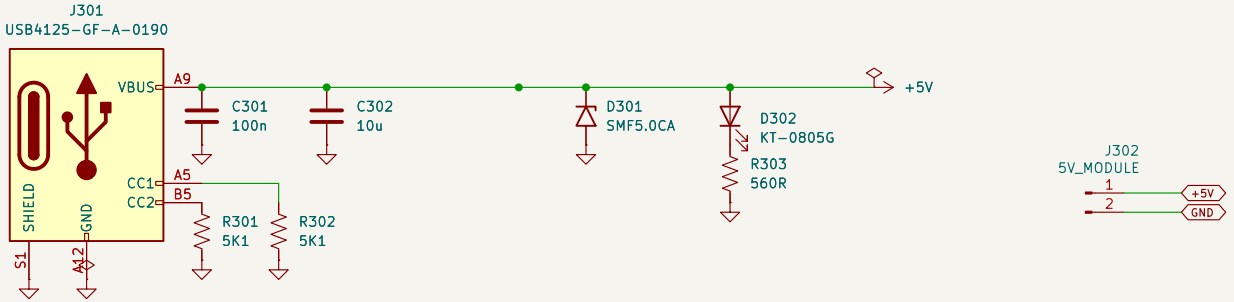
Sheet: /RPi Interface/
File: rpi_interface.kicad_sch

Title: Host module and configuration

Size: A3	Date: 2026-11-08	**Rev: 0.0.13-dev**
KiCad E.D.A. 10.0.7		Id: 2/6

USB-C 5 V input, bypass and protection

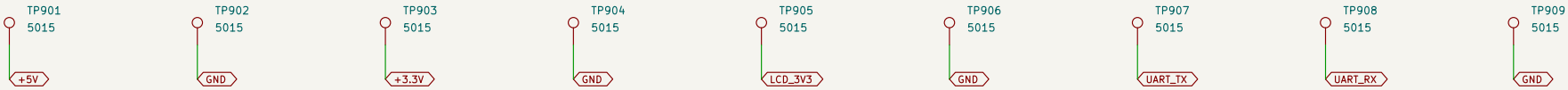
Power only: USB data is not connected. Follow +5V to the host, reader and display regulator.



USB-C sink identification
R301 / R302: 5.1 kOhm to GND
Each CC pin has its own pull-down.

Input bypass and transient protection
C301: 100 nF; C302: 10 uF
D301: SMF5.0CA TVS across the 5 V rail.

FACTORY-ASSEMBLED SERVICE POINTS: Keystone 5015 / C2906768



TP901 (+5 V), TP902 and TP909 (GND) form a 15 mm pitch front clip row: regulated 5 V bench input only. Disconnect all USB power before injection.
No source selection or reverse-polarity protection. Use current limiting; probe loops are not a strain-relieved power connector.
TP903–TP908 are in the rear service areas: 3.3 V rails, host UART and local grounds. All nine loops are factory SMT placements.

Prototype: physical fit, powered operation and assembly not qualified
Derived from 3rdIteration/SeedSigner; original design: Stephen Rothy
ShieldSigner / LightningSpore

Sheet: /Power/
File: Power.kicad_sch

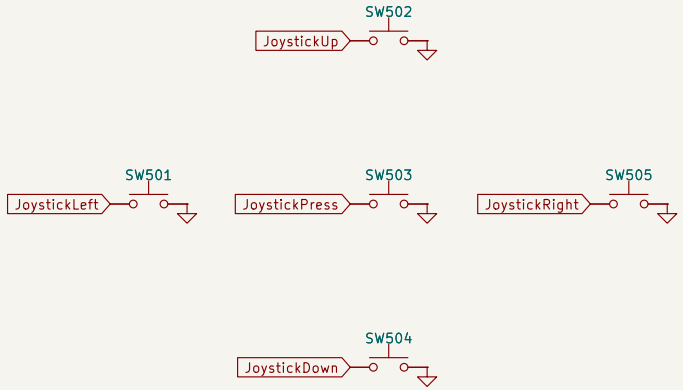
Title: USB-C power input and protection

Size: A4	Date: 2026-11-08	**Rev: 0.0.13-dev**
KiCad E.D.A. 10.0.7		Id: 3/6

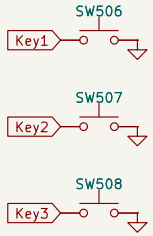
User controls: five navigation contacts + three keys

Every switch pulls its named host signal to GND when pressed. Configure host pull-ups and software debounce.
Key1 / Key2 use 1.8 V GPIO4_C0 / GPIO4_C1; other button inputs use 3.3 V. Do not pull Key1 / Key2 up to 3.3 V.

NAVIGATION



ACTION KEYS



SW501–SW508: C&K PTS636SK25SMTRLFS momentary switches.
The placement below follows the physical control arrangement. Net names match the host sheet.

Prototype: physical fit, powered operation and assembly not qualified
Derived from 3rdIteration/SeedSigner; original design: Stephen Rothy
ShieldSigner / LightningSpore

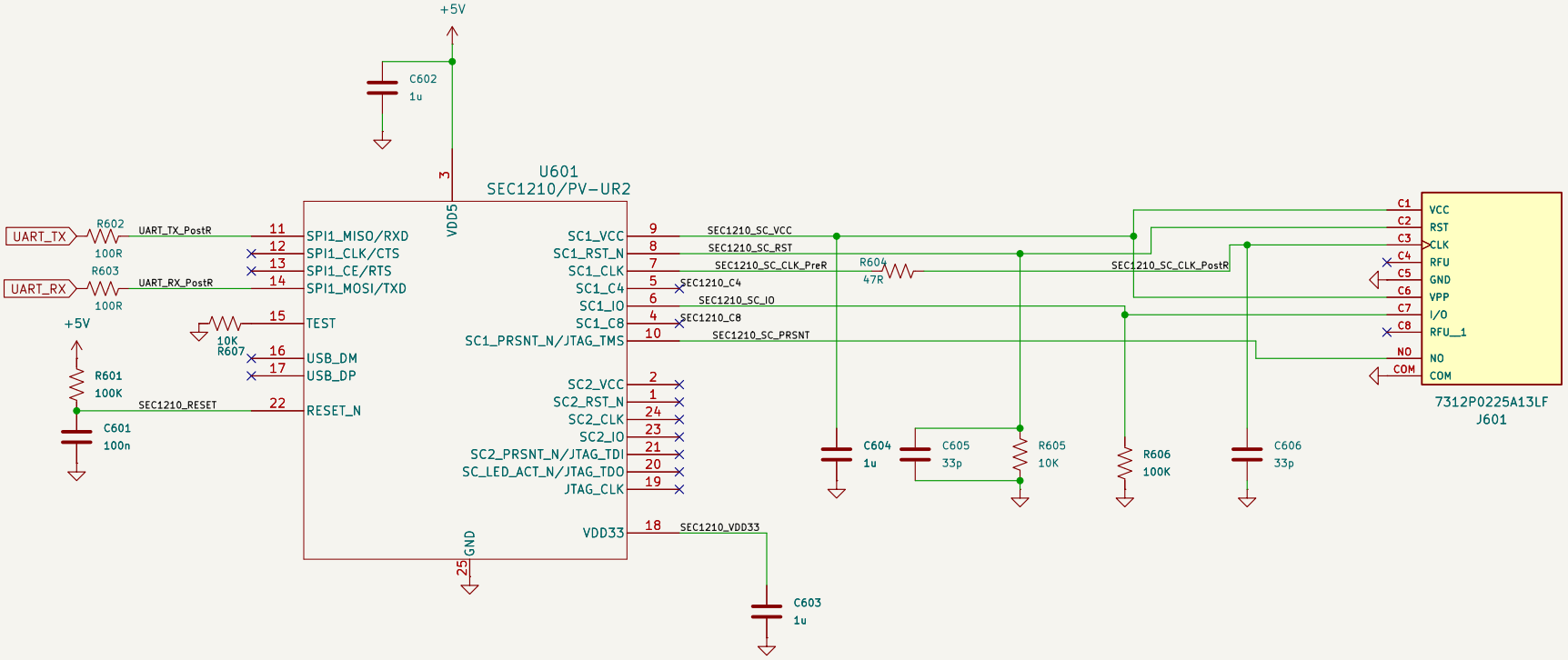
Sheet: /Buttons/
File: buttons.kicad_sch

Title: Navigation and action keys

Size: A4	Date: 2026-11-08	**Rev: 0.0.13-dev**
KiCad E.D.A. 10.0.7		Id: 4/6

SEC1210 UART reader and smartcard contacts

Host UART at left; card channel 1 at right. Channel 2, USB and JTAG pins are intentionally unused.
UART_TX is host TX to U601 RX (pin 11); UART_RX is host RX from U601 TX (pin 14).



RESET AND TEST
R601 / C601: reset pull-up and delay
R607: TEST pull-down

LOCAL BYPASS
C602: 5 V input, 1 uF
C603: VDD33 output, 1 uF
C604: card supply, 1 uF

CARD INTERFACE
R604: 47 Ohm clock series damping
C605 / C606: 33 pF; R605 / R606: bias
J601: combined SIM / full-size card socket

Prototype: physical fit, powered operation and assembly not qualified
Derived from 3rdIteration/SeedSigner; original design: Stephen Rothy
ShieldSigner / LightningSpore

Sheet: /Smartcard Interface/
File: smartcard_reader.kicad_sch

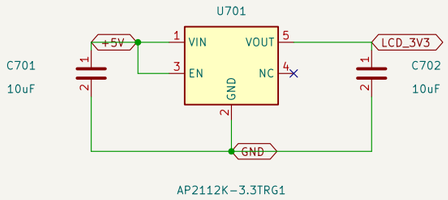
Title: SEC1210 UART smartcard reader

Size: A4	Date: 2026-11-08	**Rev: 0.0.13-dev**
KiCad E.D.A. 10.0.7		Id: 5/6

SPI display sockets and dedicated 3.3 V supply

J701 (HOTHMI / Waveshare order) or J702 (14-pin ILI9341 order) is the module header, not a 40-pin bare-panel FPC. Display power is independent of the Luckfox 3.3 V output.

DISPLAY SUPPLY

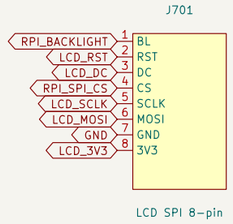


AP2112K-3.3TRG1

C701 / C702: 10 uF, 25 V X5R
Maintain at least 1 uF effective capacitance.
U701 / C701 / C702 are on the rear for service access.
Measure regulator dissipation during bring-up.

Factory straps: JP201 / JP203 / JP205 closed; JP202 / JP204 / JP206 open.
Backlight is always on. The separate PWM candidate has different hardware; see its own schematic.

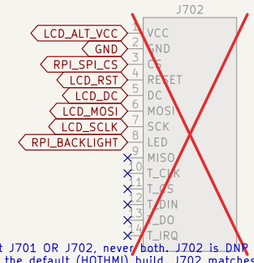
J701: CARRIER PIN NUMBERS



LCD SPI 8-pin

MODULE MATING / NUMBERING
Carrier pin 1 (BL) mates to module J1 pin 8 (BL_E).
Carrier pin 8 (3V3) mates to module J1 pin 1 (VCC).
Use the 2.54 mm J1 row, not the 2 mm J2 connector.

J702: ALTERNATE 14-PIN ILI9341



Fit J701 OR J702, never both. J702 is DNP
in the default (HOTHMI) build. J702 matches 14-pin SPI TFT modules:
VCC GND CS RESET DC MOSI SCK LED MISO + touch.
MISO and touch pins are not connected.
Firmware must select the ILI9341 driver.



J702 VCC STRAP
JP701 closed / JP702 open: LCD_3V3 (default).
JP702 closed / JP701 open: +5V, for modules
with an on-board 3.3 V regulator.
Never close both.

Prototype: physical fit, powered operation and assembly not qualified
Derived from 3rdIteration/SeedSigner; original design: Stephen Rothy
ShieldSigner / LightningSpore

Sheet: /SPI LCD + dedicated power/
File: lcd_module.kicad_sch

Title: SPI display sockets and regulator

Size: A3	Date: 2026-11-08	**Rev: 0.0.13-dev**
KiCad E.D.A. 10.0.7		Id: 6/6